Free carrier effects as a complicating variable in the analysis of strained silicon

Rajat Sharma, Matthew W. Puckett, Hung-Hsi Lin, Felipe Vallini, and Yeshaiahu Fainman¹

¹Department of Electrical & Computer Engineering, University of California, San Diego, 9500 Gilman Dr, La Jolla, CA 92023 Email: r8sharma@eng.ucsd.edu

We characterize free carrier effects in silicon waveguides due to electronic non-idealities such as dielectric fixed charges and interface states, independently considering SiO₂, SiNx and Al₂O₃ cladding layers. These effects are shown to impact both the passive and active properties of silicon waveguides.

1. Introduction

Since the first demonstration of strained silicon's second-order nonlinear susceptibility in 2006¹, substantial research has been devoted to increasing the measured coefficient in hopes of making the material a viable candidate for electro-optic modulation. Recently, values as large as 336±30 pm/V have been reported at telecommunication wavelengths, making strained silicon material platform competitive with those consisting of lithium niobate². However, many of the papers reporting values of $\chi^{(2)}$ rely on a DC characterization technique, wherein a Mach-Zehnder interferometer is operated in a push-pull configuration. In such experiments, the voltage-dependent transmission spectrum of the interferometer is used to determine the change in refractive index within each arm, which in turn gives the value of the waveguide's linear electro-optic coefficient, $\chi^{(2)}$. Although this technique may be accurate for some materials, in this work we discuss how the free-carrier effects present in such experiments, resulting from fixed interface charges and interface traps present at material interfaces, may affect the apparent electro-optic properties of a semiconductor waveguide. We conclude that these charges lead to a significant redistribution of carriers, even in the absence of an external bias, and additionally govern the value of the electric field present within the waveguide. Such effects are shown to be of particular importance in the context of capactively driven silicon devices, though they have been neglected in the literature.

2. CV measurements :To determine the fixed interface charge and interface trap density along various silicon-dielectric interfaces, we carried out C-V measurements on PECVD SiO₂ and SiN_x films on a <100> silicon substrate. Due to fabrication limitations, the corresponding values for Al₂O₃ films were taken from literature³. The flat-band voltages (V_{FB}) obtained from the two subsequently measured C-V curves, which are shown in Fig. 1, were then used to calcuate the fixed interface charges, whereas the difference in minimum capacitance between the high- and low-frequency measurements were used to determine the interface trap densities⁴. It's important to note that, while the interface of silicon with both SiO₂ and SiN_x exhibited positive fixed interface charges, thise value was negative for the case of Al₂O₃.



Fig. 1. Measured high- and low-frequency C-V measurements for SiO₂ and SiN_x films.

3. Simulations :To observe the effect of these interface charges on the behavior of silicon waveguides, we constructed models in SILVACO to separately consider each dielectric as a potential cladding material. Our simulation spaces consisted of a lightly doped (p-type, with a boron concentration of 1×10^{15} cm⁻³) silicon-on-insulator waveguide, which was 500 nm wide and 250 nm tall, clad with a 1 µm-thick layer of the dielectrics of interest. Additionally, bias voltages were applied vertically across the waveguide models to simulate the method of operation in strained silicon modulators. Fig. 2a and 2b, show the minority carrier concentration in a SiN_x-clad silicon waveguide for two bias voltages of opposite sign, indicating a noticeable redistribution of carriers between the two cases, suggesting that there will be a change in the waveguide's properties due to the free-carrier plasma dispersion effect. Moreover, we also observed a significant screening effect of the free carriers in the semiconductor region, which disallowed the applied bias voltages from having a significant impact on the electric field within the waveguide. This observation is illustrated in Fig. 2c and 2d.



Fig. 2.(a,b) Minority carrier concentrations within a silicon waveguide assuming a silicon nitride cladding and bias voltages of -10 V and 10 V, respectively. (c,d) Electric field profiles within the same waveguide assuming voltages of 0 V and 10 V, respectively.

Subsequently, the perturbations in the electron and hole concentrations for bias voltages ranging from -10 to 10V were translated into the corresponding local deviations in the value of the complex refractive index using the Soref and Bennett relations at a wavelength of $1.55 \ \mu m^5$. The real and imaginary parts of the effective index for the fundamental TE-like mode supported by each of the waveguides under consideration were then computed using the finite-difference time-domain (FDTD) solver Lumerical, and the results of this computation are shown in Fig 3.



Fig. 3. Changes in the (a) real and (b) imaginary parts of the modal effective indices for bias voltages ranging from -10 to 10 V, assuming each of the three cladding dielectrics.

As is evident, the changes in both the real and imaginary parts of the effective index are dissimilar for each of the three considered dielectrics. For the case of Al_2O_3 , it is worth further noting that the change in the real part of the refractive index can be as large as $2x10^{-5}$ for a bias of only 10 V. Given the high voltages used in the DC characterization of the electro-optic effect in strained silicon², this analysis is critical to the accurate determination of the Pockels effect, and therefore strained silicon's effective $\chi^{(2)}$. This analysis also demonstrates a non-zero value of loss, again due to the redistribution of carriers in the semiconductor, which is critical to the future characterization of passive device components.

4. Conclusion: We show that fixed interface charges at the silicon-dielectric interface can have a significant impact on the optical properties of passive and capactively driven silicon waveguides. The changes in effective index induced by carrier redistribution inside the waveguides can be comparable to those reported in literature for strained silicon making this analysis critical in their analysis. This work was supported by the Defense Advanced Research Projects Agency (DARPA), the National Science Foundation (NSF), the NSF ERC CIAN, the Office of Naval Research (ONR), the Multidisciplinary University Research Initiative (MURI), and the Cymer Corporation. Sample fabrication was performed at the UCSD Nano3 cleanroom facility.

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