Form-birefringence structure fabrication in GaAs by use of SU-8 as a dry-etching mask

Lin Pang, Maziar Nezhad, Uriel Levy, Chia-Ho Tsai, and Yeshaiahu Fainman

A thin layer of a SU-8 submicrometer pattern produced by holographic lithography was directly used as the dry-etching mask in a chemically assisted ion-beam-etching system. With optimized etching parameters, etching selectivity of 7:1 was achieved together with a smooth vertical profile. As an application, a half-wavelength retardation plate for a 1.55-μm wavelength was produced and evaluated. © 2005 Optical Society of America

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1. Introduction

Form-birefringent devices are of interest in integrated optical systems owing to the possibility of creating miniaturized polarization control devices in isotropic substrates.[1,2] However, the fabrication of such devices is not trivial in the submicrometer region, owing to the small feature size of the patterns involved. The most commonly used procedure involves preparation of the resist pattern, transfer of the pattern into a dry-etch-resistant mask layer, and then transfer of the structure into the substrate by use of dry-etching techniques. To obtain a resistant mask for the dry-etching process, one usually transfers the patterns defined by the lithography into a dielectric layer or a metal layer, followed by etching and lift-off.[2–4] Although these additional mask transfers have the potential to improve the mask durability, the process is time consuming, and the quality of the patterns may degrade owing to the complicated procedures involved in these multiple processing steps that increase the cost of the devices. Ideally, the preferred way is to use only a single resist layer for both generating the pattern and using it as the dry-etching mask for direct transfer of the pattern into the substrate. To achieve this purpose with only a single layer, one needs a high aspect ratio in the resist pattern to attain the desired depth during dry etching and to protect the upper portion of the etched profile. However, the aspect ratio decreases as the feature size is reduced because of the surface tension during the rinsing after development. Although the surface tension can be reduced by use of methods such as a less-tension rinsing solution or supercritical drying processes,[5,6] the process complexity and cost would naturally increase. On the other hand, if the parameters of the dry-etching system can be optimized to achieve sufficient etching selectivity, a thin layer of resist could be used as a dry-etching mask for transfer of the pattern, avoiding the complexity of achieving a high-aspect-ratio resist pattern.

In this paper we discuss the fabrication of a thin layer of SU-8 with a submicrometer feature size pattern by using SU-8 holographic lithography and its utilization as a dry-etching mask for transfer of the submicrometer pattern into a GaAs substrate with optimized etching parameters under the consideration of matching lateral etch and deposition rates in our chemically assisted ion-beam-etching (CAIBE) system. Section 2 describes the holographic lithography procedure to record SU-8 gratings with a rectangular profile. The optimization of pattern transfer from a thin layer of a submicrometer pattern into a GaAs substrate is discussed in Section 3. In Section 4 we demonstrate the applicability of this approach by considering the example of a half-wave retardation plate. Conclusions are given in Section 5.

2. Holographic Lithography and SU-8 Gratings with a Rectangular Profile

An Ar^+-ion laser operating at a UV wavelength of 364 nm is used as the illumination source in our holographic lithography system.[7,8] The beam derived

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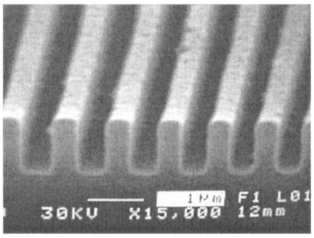
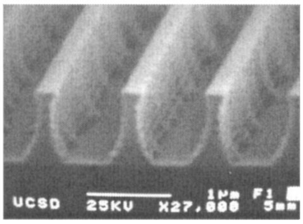
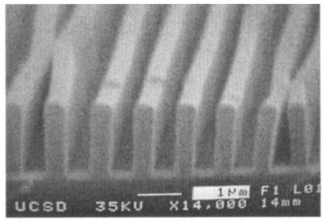


(a)

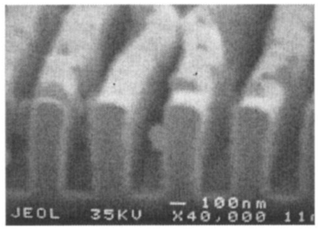


(b)

Fig. 1. SEM photographs of gratings with period of 1 μm produced by holographic lithography: (a) SU-8 gratings with a thickness of approximately 1 μm, duty cycle of 0.4, and aspect ratio of 2.4 and (b) BPRS-100 resist gratings with a thickness of 0.8 μm.



(a)



(b)

Fig. 2. Collapse of the SU-8 pattern: (a) 1-μm period with a thickness of 1.7 μm and aspect ratio of 3.7 and (b) 400-nm period with an aspect ratio of 3 with some SU-8 residue left on the surface.

from the laser source is expanded and collimated, then split into two beams with a nonpolarizing UV beam splitter. The two beams are then reflected onto the sample at an angle that can be adjusted to achieve the desired period, $\lambda/2\sin(\theta/2)$, where λ and θ are the wavelength of the laser and angle between the two beams, respectively.

Two types of resist were investigated for patterning the rectangular profile: SU-8 and BPRS-100. SU-8 resist (MicroChem Corp.) was spin coated on cleaned GaAs substrates. A soft prebake process was performed at a temperature of 95 °C for 10 min to remove all the solvent in the SU-8 layer. After the exposure, the sample is baked in an oven, in a postexposure bake (PEB) step for cationic photopolymerization of the epoxy. The SU-8 is then developed in propylene glycol methyl ether acetate, rinsed in a solvent of isopropyl alcohol, and then dried in air. Figure 1(a) shows the scanning electron microscopy (SEM) photograph of fabricated SU-8 gratings with a period of 1 μm, thickness of 1 μm, duty cycle of 0.4 (defined as the ratio of the grating ridge width to the period), and aspect ratio of 2.4 (defined as the ratio of the grating ridge width to the thickness). From Fig. 1(a), it can be seen that the sidewall of the grating structure is vertical and smooth.

For comparison, BPRS-100 (OCG Microelectronic Materials), a positive photoresist, was used in the same setup. After it is cleaned and hexamethyldisilazane primed the GaAs wafer is spin coated with the resist followed by a 20-min prebake at 110 °C. After exposure, the wafer is developed in PLSI developer diluted to PLSI:water = 1:3 for 60 s. Figure 1(b) shows the SEM photograph of a BPRS-100 grating with thickness of 0.8 μm. It can be seen that the profile of the pattern has a sinusoidal nature as opposed to the rectangular profile in SU8. Furthermore, a standing-wave structure on the sidewall of the grating can be seen clearly, which is attributable to the high reflectivity of the GaAs substrate.[9] Although the standing-wave structure can be overcome by use of antireflective coatings on the bottom of the photoresist,[9] the shape of the profile cannot be further improved, indicating that BPRS-100 resist, a low-contrast photoresist, is probably not ideal for the production of rectangular profile patterns with holographic lithography with submicrometer features.

In contrast, SU-8 is a chemically amplified cross-linking resist, so the exposure generates only induced acid (i.e., Lewis acid), and an acid-catalyzed cross-linking is enhanced in PEB. Thus one can obtain a thick SU-8 pattern layer (up to several hundred micrometers) in microelectromechanical system fabrication.[10] Additionally, SU-8 is a high-contrast resist (i.e., there is a sharp jump to reach the illumination level required for exposure). Therefore the pattern profile in SU-8 is binary (step profile), which is less sensitive to fluctuations of the illuminated intensity, eliminating the effect of the standing waves on its profile.

The thickness of the SU-8 layer is dominantly determined by the spin speed. By decreasing the spin speed, one can increase the aspect ratio of the structure. However, the collapse of the structure would become a major issue. The collapse is shown in Fig. 2(a), in which the 1.7-μm-thick grating has a 1-μm period with a duty cycle of 0.45 and aspect ratio of 3.7. The phenomenon becomes even worse with the decrease of the feature sizes (as required for telecommunication wavelength applications). An example is shown in Fig. 2(b), in which the period of the col-

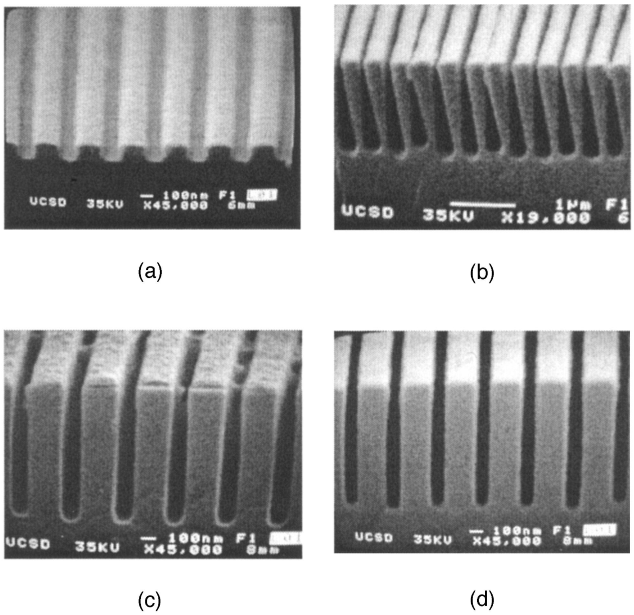


Fig. 3. SEM photographs of submicrometer gratings: (a) SU-8 mask with a 350-nm period and aspect ratio of 0.6, (b) transferred structure in GaAs with an inverse taper profile by use of the thin-layer SU-8 (a) as the dry-etching mask, (c) improved but contaminated profile, (d) smooth and vertical sidewall structure in GaAs with an aspect ratio of 4 and thickness of 950 nm.

lapsed structure is approximately 400 nm with a duty cycle of 0.5 and aspect ratio of 3.

The pattern collapse is primarily due to the capillary force that occurs during the drying after development. One way to suppress the collapse and the distortion of the small feature size structures is to reduce the surface tension of the rinse solution,[5] which we are currently investigating via supercritical resist drying methods.[6]

Elimination of the wavy feature in the grating structure can be achieved by decreasing either the surface tension of the drying process or the thickness of the resist (i.e., reducing the aspect ratio of the structure). Gamma butyrolactone was used to dilute the SU-8 2 resist to 1:1 in volume ratio, and a spin speed of 3000 revolutions per minute was used to achieve a thin and uniform layer on the GaAs substrate. With suitable exposure and PEB, a thin submicrometer structure can be produced. Figure 3(a) shows a structure having a period of approximately 350 nm, duty cycle of 0.6, thickness of 130 nm, and aspect ratio of 0.6. Our goal is to utilize the small aspect ratio pattern as a dry-etching mask while optimizing CAIBE parameters to accomplish the desired etch depth and grating profile in the GaAs substrate.

As mentioned above, wavy structures are observed after development, which is attributed to weak cross-linking and surface tension during the rinsing process. High exposure dosage can improve the quality of the result. However, the duty cycle will increase with the increase of exposure dosage owing to sinusoidal distribution of interference intensity in the holographic pattern and the diffusion mechanism of induced acid during the PEB procedure. Nevertheless, for too high exposure, the standing wave originating from the high reflectivity of the substrate surface will begin to affect the smoothness of the sidewall. To avoid this, we utilized the nonlinearity of the PEB process (which we have previously investigated for large feature sizes[7]) to achieve the desired structure.

3. Transfer of the Submicrometer Grating into GaAs

The GaAs wafer with the developed SU-8 structure is mounted on the wafer chuck in the vacuum chamber by a load-lock chamber in our CAIBE system, which is equipped with a 12-cm inductively-coupled-plasma rf source with two self-aligned grids, a screen grid and an accelerator grid. The wafer chuck is located 50 cm from the grids. The maximum beam and voltage accelerator voltages are 2000 and 500 V, respectively. Typical values of the beam and acceleration voltages range from 300 to 750 V and from -25 to -500 V, respectively, depending on the etched structures. The base pressure of the vacuum chamber is pumped down to the low 10^{-8} Torr scale, and the typical chamber pressures during an etching process range from approximately 0.10 to 0.8 mTorr. The sample stage is water cooled to control the temperature of the wafer during etching.

In our CAIBE, chlorine (Cl_2) is used as a chemical etching gas with argon gas as the plasma ion (Ar^+) source. The etching rate and profile are influenced by the combined effect of various parameters in the system, such as beam voltage, accelerator voltage, beam current, substrate temperature, chamber pressure, gas flow of Cl_2, and substrate material. Under the etching parameters of beam voltage of 400 V, accelerator voltage of 425 V, Cl_2 gas flow of 10 SCCM (SCCM denotes cubic centimeters per minute at STP), Ar gas flow of 10 SCCM, beam current of 40 mA, and substrate temperature of 5 °C, a vertical sidewall profile was achieved for a 1-μm-period grating structure,[7] with the etching rate selectivity being approximately 3:1. With these etching parameters, we have previously succeeded in transferring a photonic crystal structure with hexagonal periodic patterns and defect lines into a GaAs substrate.[8] However, these etching parameters are not suitable for the thin mask layer as shown in Fig. 3(a) because the maximum achievable depth is only approximately 400 nm, and because of the damage to the upper portion of the etched structure due to mask erosion. At this juncture, instead of attempting to complicate the process by producing a high-aspect-ratio SU-8 layer or by transferring the pattern into harder material, such as an etch-resistant metal or a silicon dioxide layer, we chose to optimize the CAIBE parameters to increase the etching selectivity for our application purpose.

To increase the etching selectivity, we reduce the Ar gas flow into the plasma generator to 7 SCCM to lower the Ar^+-ion density for decreasing the erosion rate of the SU-8 resist; meanwhile the chuck temperature is raised to 20 °C to increase the etching rate of GaAs while the beam voltage (400 V), acceleration voltage (425 V), and beam current of 40 mA are kept constant. Most importantly, the lateral etch rate should match the lateral deposition of created residue to achieve a vertical and smooth sidewall, so the Cl_2 gas flow is adjusted to investigate its effect on the etched sidewall profile.

Figure 3(b) shows the etched result by use of a Cl_2 flow of 18 SCCM, corresponding to a chamber pressure of 0.60 mT. Because there is no throttle valve in our system, the pressure cannot be controlled independently. As shown in Fig. 3(b), the etched profile is an inverse taper with a decrease of the duty cycle from approximately 0.6 in the upper portion to 0.2 in the bottom portion. This structure is unstable and thereby collapses. The inverse taper shape indicates that the lateral etching rate is higher than the deposition rate of the reactants, which one could improve by raising the deposition rate to protect the sidewall with an increase of Cl_2 gas flow while keeping other parameters unchanged as shown in Fig. 3(c). From Fig. 3(c), at a Cl_2 gas flow of 20 SCCM, it can be seen that the etched sidewall is almost vertical; however, some residues are left in the grating grooves, which probably originate from the contaminations in the chamber. A cleaning procedure was conducted to eliminate the contamination by Ar^+ plasma for approximately 1 h before the above process was repeated. Clean grating grooves and sharply etched smooth sidewalls were achieved as shown in Fig. 3(d), in which the etch depth is approximately 950 nm with an aspect ratio of approximately 4. The erosion rate of the SU-8 resist layer and the etching rate of GaAs are 3 and 23 nm/min, leading to the etching rate selectivity of more than 7:1. There is still some SU-8 residue left on the surface, which can be removed by the plasma asher.[7] Figure 3(d) also shows that the upper portion of the etched pattern remains quite square in profile, indicating that the described optimized etching procedure is a damage-free process, which could previously be achieved only by thick resist or hard mask transfer.[11,12]

Note that, in this optimized process, the anisotropic etch is accomplished by one's increasing the lateral deposition rate to match the lateral etching rate. These two rates processes can also be matched by reduction of the lateral etching rate, which we are currently investigating.

4. Form-Birefringence Retardation

The goal of the preceding etch procedure is to present an easy and efficient way to produce a deep periodic nanostructure in a GaAs substrate. As an illustrative example, we describe the results of fabricating a form-birefringent half-wave retardation plate for the wavelength of 1550 nm in GaAs with the described etching process. The retarder design was performed with rigorous coupled-wave analysis (RCWA).[13–15] Figure 4 shows the expected phase retardation versus the grating height, assuming a duty cycle of 0.70, grating period of 325 nm, and substrate index of 3.37.

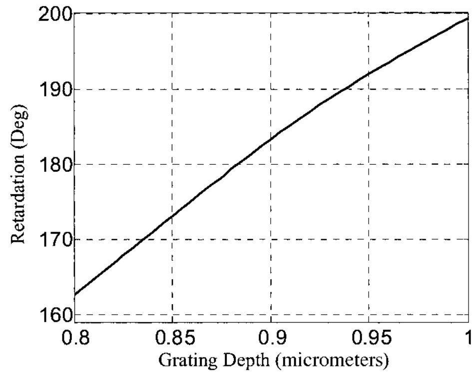


Fig. 4. RCWA-generated curve showing the effect of etch depth on the total retardation of a grating etched in GaAs at 1550 nm (n = 3.37). The nominal duty cycle and grating period are assumed to be 0.70 and 325 nm, respectively. Half-wave retardation is obtained for a grating depth of 880 nm.

Half-wave retardation can be achieved with a grating height of 880 nm. Nevertheless, the simulation results ignore substrate reflections. This is justified only if an antireflection coating layer is applied to the back side of the substrate. With no antireflection coating, the retardation is expected to oscillate with the substrate thickness owing to multiple substrate reflections.[16] Figure 5 shows the expected phase retardation for a grating depth of 880 nm and duty cycle of 0.70, where the substrate thickness is allowed to vary. The phase retardation is oscillating from 172.5 to 187.5. Typically, the oscillation is undesired as it imposes a limit on the achievable retardation accuracy. Nevertheless, one can take advantage of this characteristic to compensate for fabrication errors by thermal tuning of the device.

On the basis of the theoretical curve (see Fig. 4) we fabricated a sample by using the fabrication procedure described in Section 3. The retardation was then measured with an ellipsometric setup.[16] To obtain thermal tuning, we mounted the sample onto a Peltier thermoelectric cooler (Melcor) and adjusted the operating temperature by using a temperature controller (McShane Model 5C7-195). Figure 6 shows the

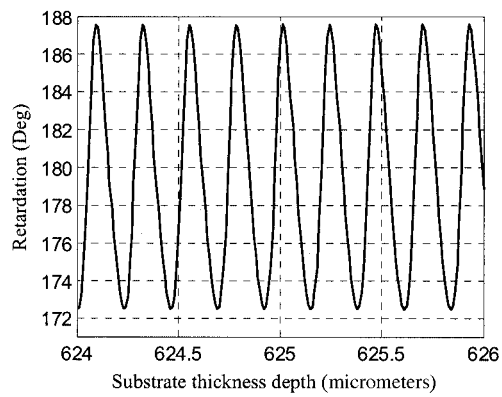


Fig. 5. Variation in retardation versus the substrate thickness with no antireflection coating on the back side for a grating depth of 880 nm and duty cycle of 0.70.

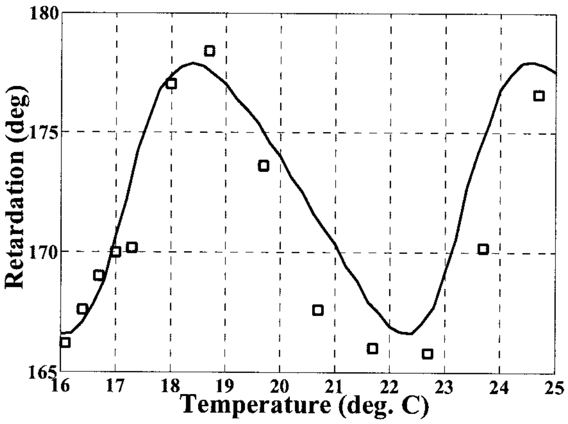


Fig. 6. Variation in retardation of the fabricated sample versus temperature (rectangular markers) and fitted theoretical curve obtained with RCWA. The fitted grating is having a duty cycle, period, and etch depth equal to 0.71, 325 nm, and 850 nm, respectively.

results obtained by temperature tuning of the sample (rectangular marks). For comparison, a theoretical curve obtained with RCWA analysis of the temperature effects is given as well (solid curve). We obtained the RCWA results by taking into account the variation of the optical path with temperature (resulting both from thermal expansion and from index variation with temperature). This combined effect was measured with a reference substrate and found to be of the order of 0.127 μm/°C. In addition, we varied the duty cycle and the grating depth to best fit the measured results. From the fitted data, the actual etch depth and duty cycle of the sample were found to be 850 nm and 0.71. This explains the slight discrepancy between the average measured retardation (172°) and the desired half-wave retardation.

5. Conclusion

A thin layer of a SU-8 submicrometer pattern produced by holographic lithography was used as the dry-etching mask in a CAIBE system. With the optimized etching parameters, etching selectivity up to 7:1 has been achieved with vertical and smooth sidewalls and a damage-free upper portion of the etched profile. A submicrometer form-birefringent structure, with a period of 325 nm, was fabricated to achieve a temperature-tunable half-wave retardation plate in GaAs at the wavelength of 1.55 μm.

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